VERSION WITH MARKINGS TO SHOW CHANGES MADE

1. (AMENDED) An apparatus coupled to a low speed tester and a device having a first speed faster than a second speed of said low speed tester, wherein said apparatus is configured to allow said low speed tester to perform high speed tests of said device at said first speed.

12. (AMENDED) The apparatus according to claim 4, wherein said apparatus is further configured to receive and verify [said] one or more transmitted test packets.

15. (AMENDED) An apparatus comprising:

means for testing a device having a first speed; and

means for configuring a low speed tester having a second speed slower than said first speed to perform high speed tests of said device at said first speed through said testing means.

16. (AMENDED) A method for testing [a device] comprising the steps of:

(A) testing a device having a first speed with a host emulator; and

(B) configuring a low speed tester having a second speed slower than said first speed to perform high speed tests of said device at said first speed through said host emulator.

18. (AMENDED) The method according to claim [15] 16, wherein step (B) further comprises:

configuring said low speed tester to control [a] said host [emulation] emulator.

R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

The present invention concerns an apparatus coupled to a low speed tester and a device. The device may have a first speed faster than a second speed of the low speed tester. The apparatus may be configured to allow the low speed tester to perform high speed tests of the device at the first speed.

SUPPORT FOR THE CLAIM AMENDMENTS

Support for the claim amendments can be found on page 15 line 16 through page 16 line 6 and FIG. 3, as originally filed. Thus, no new matter has been added.

OBJECTION TO THE DRAWINGS

The objection to the FIG. 2 has been obviated by appropriate resizing and should be withdrawn. The objection to FIG. 3 has been obviated by appropriate amendment to the specification and should be withdrawn.

OBJECTION TO THE SPECIFICATION

The objection to the specification has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §112

The rejection of claims 12, 18 and 19 under 35 U.S.C. §112, second paragraph, has been obviated by appropriate amendment and should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 1, 3-8 and 15-19 under 35 U.S.C. §103(a) as being obvious over Hannah '581 in view of Chakradhar et al. '373 (hereafter Chakradhar) has been obviated in part by appropriate amendment and is respectfully traversed in part and should be withdrawn.

The rejection of claims 2 and 9-12 under 35 U.S.C. §103(a) as being obvious over Hannah '581 in view of Chakradhar '373 and in further view of Chew '260 is respectfully traversed and should be withdrawn.

The rejection of claims 13, 14 and 20 under 35 U.S.C. §103(a) as being obvious over Hannah '581 in view of Chakradhar '373 and in further view of Jenkins et al. '868 (hereafter Jenkins) and U.S. patent Application Publication No. 2002/011516A1 to Lee is respectfully traversed and should be withdrawn.

Hannah teaches an apparatus and method for operating a peripheral device as either a master device or a slave device (Title). Chakradhar teaches a system and method for testing high speed VLSI devices using slower testers (Title). In contrast,

pending claim 1 (apparatus), 15 (means), and 16 (method) provide configuring a low speed tester to perform high speed tests of a device. The Office Action does not meet the burden of proof that it would be obvious to combine the teachings of Hannah with the teachings of Chakradhar. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Three criteria are required to establish a prima facie case of obviousness. The Examiner must show that (1) there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references, (2) there is a reasonable expectation of success, and (3) the prior art reference (or combination of references) teaches or suggests all of the claim limitations (M.P.E.P. §2142). The Court of Appeals for the Federal Circuit has indicated that the requirement for showing the teaching of motivation to combine references is "rigorous" (In re Anita Dembiczak and Benson Zinbarg, 50 U.S.P.Q.2d 1614 (Fed. Cir. 1999)). Moreover, this showing, which is rigorously required, must be "clear and particular" (Dembiczak at 1617). It is well established that merely because references can be combined, the mere suitability for logical combination does not provide motivation for the combination (See, Berghauser v. Dann, Comr. Pats., 204 U.S.P.Q. 398 (DCDC 1979); ACS Hospital Systems, Inc. v. Montefiore Hospital,

221 U.S.P.Q. 929 (Fed. Cir. 1984)). Moreover, mere conclusory statements supporting the proposed combination, standing alone are not "evidence" (McElmurry v. Arkansas Power & Light Co., 27 U.S.P.Q.2d 1129, 1131 (Fed. Cir. 1993)). Furthermore, ACS Hospital Systems indicates that an Examiner may not use the patent application as a basis for the motivation to combine or modify the prior art to arrive at the claimed invention.

Assuming, *arguendo*, that the combination would have been obvious to one or ordinary skill in the art (for which Applicants' representative does not necessarily agree), the suggested combination does not teach or suggest every element as arranged in the pending claims. In particular, claim 1 provides an apparatus coupled to a low speed tester and a device. Pending claims 1, 15 and 16 provide high speed tests of the device through an apparatus/ testing means/host emulator. In contrast, page 5, paragraph 10, lines 4-11 of the Office Action refer to a Universal Serial Bus (USB) master device of Hannah as a host emulator. Page 6, lines 12-15 of the Office Action associates the host emulator with the test generator 10.1 of Chakradhar. However, FIG. 10 of Chakradhar shows that the test generator (USB master device) does not interface with the tested circuit 10.2 (USB slave device). FIG. 10 of Chakradhar also shows that the tested circuit 10.2 (USB slave device) is tested in part through an input vector block 10.3 and in part directly by the slow tester 10.1. If the USB master device of

Hannah is the test generator of Chakradhar, the interface between the USB master device and the USB slave device is broken, contrary to the teachings of Hannah. Therefore, the suggested combination of Hannah and Chakradhar does not appear to teach or suggest an apparatus coupled to a low speed tester and a device nor high speed tests of the device through the apparatus/means for testing/host emulator as presently claimed.

Furthermore, if the USB master device of Hannah is the input vector block 10.3 of Chakradhar, then input vector block 10.3 would have bidirectional interfaces to (i) the tested circuit 10.2 and (ii) to the slow tester 10.1 to support the master/slave bus traffic contrary to the unidirectional interfaces taught by Chakradhar. In contrast, Chakradhar does not appear to teach or suggest that the slow tester 10.1 can receive data from the tested circuit 10.2 through the input vector block 10.3. Therefore, Hannah and Chakradhar alone and in combination do not appear to teach or suggest high speed tests of the device through the apparatus/means for testing/host emulator as presently claimed. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

The Office Action does not provide clear and particular evidence that there is some suggestion or motivation, either in the references or in the knowledge generally available to one of ordinary skill in the art, to modify or combine the references.

Hannah appears to be silent on testing devices. Therefore, Hannah does not appear to teach or suggest an apparatus allowing tests of a device as presently claimed. As such, there is no motivation or suggestion by Hannah to seek the teachings of Chakradhar to implement an apparatus or low speed tester for such tests.

Furthermore, Chakradhar appears to be silent on testing the tested circuit 10.2 indirectly through an apparatus. At best, Chakradhar may suggest testing of the combined master/slave system taught by Hannah as the tested circuit 10.2, but not testing of just the slave device remotely through the master device. Therefore, Chakradhar does not appear to teach or suggest high speed tests of a device through an apparatus/testing means/host emulator as presently claimed. As such, there is no motivation or suggestion by Chakradhar that the device taught by Hannah could be tested through the another device.

Furthermore, the Office Action does not provided any additional evidence that the suggested combination would be motivated or suggested by knowledge generally available to one of ordinary skill in the art. Therefore, there is no clear and particular evidence of suggestion or motivation to combine the references. As such, the Office Action does not make a prima facie case that the combination would be obvious and the rejection should be withdrawn.

The Office Action does not provide clear and particular evidence that there is a reasonable expectation of success for the suggested combination. The increased fault coverage and reduced application time cited in Chakradhar may apply to the configuration taught by Chakradhar, but no evidence has been provided in the Office Action that an increased fault coverage or reduced application time would be experienced in the suggested combination. In particular, FIG. 10 of Chakradhar teaches that the slow tester 10.1 has direct access to the tested circuit 10.2 to observe output signals from the tested circuit 10.2. In contrast, modifying the master/slave system of Hannah with Chakradhar would place the master device between the slow tester 10.1 and the tested circuit 10.2 No evidence is provided by the Office Action that the slow tester 10.1 would still be able to provide increased fault coverage or reduced application time if forced to observe the tested circuit 10.2 through the master device of Hannah. Thus, there is no clear and particular evidence that there is a reasonable expectation of success for the suggested combination. Therefore, the Office Action does not make a prima facie case that the combination would be obvious. As such, the present invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 2 and 9-12 depended either directly or indirectly from independent claim 1, which is now believed to be allowable.

As such, the presently pending invention is fully patentable over the cited reference and the rejection should be withdrawn.

Claims 13, 14 and 20 depended either directly or indirectly from independent claims 1 or 16, which are now believed to be allowable. As such, the presently pending invention is fully patentable over the cited reference and the rejection should be withdrawn.

Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

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